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JACKPOT APPARATUS

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(56) Prior Art Documents
AU 628954 82448/90 G07F 17/34
AU 53370/86 G07F 17/34
AU 543997 75784/81 G07F 17/34

(57) Claim

1. A random payment awarding apparatus for connection to a plurality of poker machines each adapted to produce an incrementing signal at each operation thereof, said apparatus including means to generate and store a random number within a predetermined range; counting means adapted to increment through the numbers in said range and responsive to incrementing signals from each said poker machine; first comparator means to compare said random number and the number held in said counting means; means responsive to said first comparator means for recording the identity of the poker machine which produced the last incrementing signal if said random number and the number held in said counting means are equal; display means to display a number held in said counting means after each increment and/or a prize award

../2

indication, and the identity of the poker machine which produced the last incrementing signal if said random number and the number held in said counting means are equal, said apparatus further including timing means for determining when a rate at which said incrementing signals are received falls below a selected minimum value; and second comparator means responsive to the timing means for providing an indication when the counting means holds a number differing from the random number by less than a predetermined amount when the rate at which the poker machines are played is below said minimum value.

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AUSTRALIA

PATENTS ACT 1990

COMPLETE SPECIFICATION

FOR A STANDARD PATENT

ORIGINAL

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Invention Title: "JACKPOT APPARATUS"

Details of Associated Provisional Application No: PK5211

The following statement is a full description of this invention, including the best method of performing it known to me:-

The present invention relates to an apparatus for use with poker machines and, in particular, to an apparatus for awarding additional prizes to poker machine players.

Much of the art of managing poker machines involves the encouragement of players by novel variations in the schemes of playing and awarding prizes. Preferably such schemes involve minimum modification of the poker machine hardware. Frequently this is done at the expense of increased administrative complexity and additional staff.

It is an object of the present invention therefore to provide a random payment awarding apparatus which will overcome, or at least ameliorate, the disadvantages of the prior art.

According to the present invention there is provided a random payment awarding apparatus for connection to a plurality of poker machines each adapted to produce an incrementing signal at each operation thereof, said apparatus including means to generate and store a random number within a predetermined range; counting means adapted to increment through the numbers in said range and responsive to incrementing signals from each said poker machine; first comparator means to compare said random number and the number held in said counting means; means responsive to said first comparator means for recording the identity of the poker machine which produced the last incrementing signal if said random number and the number held in said counting means

are equal; display means to display a number held in said counting means after each increment and/or a prize award indication, and the identity of the poker machine which produced the last incrementing signal if said random number and the number held in said counting means are equal, said apparatus further including timing means for determining when a rate at which said incrementing signals are received falls below a selected minimum value; and second comparator means responsive to the timing means for providing an indication when the counting means holds a number differing from the random number by less than a predetermined amount when the rate at which the apparatus is played is below said minimum value.

Preferably, the random number is indicative of an amount of money which is paid to the player operating the machine which produced the last incrementing signal.

A preferred embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a schematic block diagram of the circuitry of the random payment awarding apparatus;

Figures 2 and 3 together form a circuit diagram of the processor portion shown schematically in Figure 1;

Figures 4 and 5 together form a circuit diagram of the poker machine interface shown in Figure 1; and

Figures 6 and 7 together form a circuit diagram of the display interface shown in Figure 1.

Referring now to Figure 1, the random payment awarding apparatus 1 includes a processor portion 2 and interfaces 3, 4 to a display 5 and a number of poker machines 6 respectively. Power 7 is distributed to each portion. The processor portion includes means (not shown) for generating and storing a random number. The random number generator is essentially a free running clock and associated counter started by a reset of the system and stopped after an indeterminate interval by a first operation of one of the poker machines. At this point the counter associated with the clock contains a random number. Counting means are provided for counting operations of the poker machines. A prize is awarded when the counting means contains a value equal to the random number generated previously. In addition, the rate at which the poker machines are played is compared to a predetermined value. When the rate of play is less than the predetermined value, the value held by the counting means is compared to the random number and if it is found to be within a predetermined amount of the random number, an indication is provided in the form of audio and visual encouragement to the players.

Referring now to Figures 2 and 3, the processor portion is shown in greater detail. Lines A and B at the bottom right hand corner of Figure 2 continue on Figure 3. Power for the circuitry is derived from an AC supply by means of a bridge rectifier D4 to D7 and 7805 three terminal regulator UB. An intermediate 12 volt DC supply

is used both to charge a 3.6 volt back-up battery and to supply devices external to the processor portion. The back-up battery supplies memory devices so that data may be retained when power is not available from the AC supply.

A 6802 microprocessor UB executes a program stored in one or more 2716 EPROMs UC, UD with a 6116 RAM UE for storage of intermediate results. It will be noted that the 6116 device is connected to the battery. The microprocessor is reset upon application of power to the circuit due to the NE 555 timer UH configured as a monostable and triggered from the 12 volt supply. A 6821 peripheral interface adaptor UA allows the microprocessor to control external devices through an edge connector J1. The microprocessor communicates with other equipment via a 6850 asynchronous communications interface adaptor UF and associated serial interface J2. Addressing of all these peripheral devices as memory is accomplished by address decoders UM driven by the microprocessor. In addition, a CD4020 binary counter UN counts clock pulses from the microprocessor to generate regular interrupt pulses via the peripheral interface adaptor. These interrups are essential to the operation of software executed by the microprocessor, as will be described hereafter.

Figures 4 and 5 show the interface responsive to the stroke meters (not shown) of substantially conventional poker machines. The ten address lines at

the right hand side of Figure 4 continue on Figure 5. Up to thirty poker machines are accommodated by the circuitry of Figure 5. The peripheral interface adaptor UA of Figure 2 receives signals from the solenoids of the poker machines' stroke meters multiplexed via several CD4052 analog switches U32 to U35 and a 74HC540 buffer U31. The solenoid signals pass through bridge rectifiers B20 to ensure that the polarity is appropriate to drive 4N35 optocouplers U20. The optocouplers electrically isolate the poker machines from the circuitry of the invention in order to avoid errors which may be caused by earth loops, for example. The counter incremented on receipt of these poker machine signals may be incremented by any suitable amount, stored in EPROM. The counter value is also interpreted as an amount of money. Because the microprocessor controls the multiplexing of the analog switches, it is able to identify the source of an incrementing signal. Figure 5 shows only one of these optocouplers U20 but each input from a poker machine is similarly equipped.

Figure 4 also includes an interface connector J3 allowing operator control of the random payment awarding apparatus. Two switches (not shown) are connected to the peripheral interface adaptor of Figure 2 via a pair of optocouplers U7 and U8 and the 50-pin connector shown at the left hand side of both Figures 2 and 4. Inductors L1, L2 and capacitors C9, C10 in series with the signals filter high frequency noise which may arise when the

switches are located remotely from the apparatus. A further switch is connected to the peripheral interface adaptor via the connector J3 but is not available for remote operation. The three switches allow up to 8 processor functions to be initiated for diagnostic and auditing purposes.

A pair of power transistors TR1, TR2 driven by the peripheral interface adapter permits the connection of annunciator lights for alerting poker machine operators to the proximity of a prize 'pay-off'.

Figures 6 and 7 show the display interface which includes a second 6821 type peripheral interface adaptor U1 communicating via edge connector J4 with the processor portion. The peripheral interface adaptor U1 drives a number of CD4099 addressable latches for control of an LED matrix (not shown) through a corresponding number of ULN2003 transistor arrays. The uppermost CD4099 and ULN2003 pair U2 and U6 drives the seven rows of the LED matrix while the remaining pairs drive the five columns. The current sourcing capacity of the row drivers is enhanced by the use of higher power transistors TR1 to TR7. The LED matrix is connected to the circuitry of Figure 7 by ribbon cable at a pair of edge connectors J5, J6.

Continuous operation of the microprocessor (executing a suitable routine) is necessary to sustain a complete display on the LED matrix. In this way a processor malfunction is unlikely to cause the display of

incorrect prize formation. In addition, a single bit output AUDE of the second peripheral interface adaptor U1 provides an audio signal under program control for driving a loudspeaker or similar transducer.

In use, the 6802 microprocessor UB is reset by a signal generated by the NE 555 timer UH on the application of power to the system. The microprocessor emulates the free running clock and associated counter mentioned previously. Under software control the microprocessor increments an internal register or memory location, cycling between numbers representative of minimum and maximum pay out of the prize award. At the first operation of a poker machine an interrupt is generated by the peripheral interface adaptor UA which informs the microprocessor to stop counting and regard the value of the count as the random number. This value is later interpreted as the amount of the prize awarded.

Thereafter, operation of the poker machine is detected by polling the multiplexed solenoid signals within an interrupt routine called by interrupts from the CD4020 counter UN. Each poker machine is assigned a weighted value, stored in EPROM UC or UD. The weighted values represent fractions of a cent in proportion to the denomination of the coins or tokens used in the poker machines and the percentage of the 'pay-in' returned to players as the prize. Operation of the poker machines causes the weighted values to be acccumulated until the value includes an integer portion. The integer portion

is used to increment a further memory location and the fractional portion continues to be accumulated. The contents of the memory location are compared to the prize amount.

The microprocessor adds the value in the memory location to a predetermined amount or 'lookahead', stored in EPROM. When this total equals or exceeds the random number also stored by the microprocessor the rate at which the poker machines are being played is compared to a predetermined value.

The rate of play is calculated with respect to the timing information generated by the CD4020 regular interrupts discussed above. If the rate is less than the predetermined value stored also in EPROM the LED matrix is driven by the microprocessor to indicate proximity to the additional prize jackpot. In addition, audio signals are generated to further encourage players. If however the rate at which the poker machines are played is equal to or above the predetermined value no indication is necessary.

When further playing of the poker machines increments the memory location until it is equal to the random number previously generated, the processor drives the LED matrix to indicate that the prize jackpot has been won by the player of the last poker machine to increment the counter. The amount of the prize is the value of the random number. The system must be reset before play continues. This is performed by authorised

personnel using the switches interfaced to connector J3 of Figure 4.

By incorporating the various predetermined values employed by the processor within read only memory, it will be appreciated that tampering with the system to promote jackpot payouts is prevented or at least discouraged. It will also be apparent that, while the invention has been described with reference to specific examples, it may be embodied in many other forms.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. A random payment awarding apparatus for connection to a plurality of poker machines each adapted to produce an incrementing signal at each operation thereof, said apparatus including means to generate and store a random number within a predetermined range; counting means adapted to increment through the numbers in said range and responsive to incrementing signals from each said poker machine; first comparator means to compare said random number and the number held in said counting means; means responsive to said first comparator means for recording the identity of the poker machine which produced the last incrementing signal if said random number and the number held in said counting means are equal; display means to display a number held in said counting means after each increment and/or a prize award indication, and the identity of the poker machine which produced the last incrementing signal if said random number and the number held in said counting means are equal, said apparatus further including timing means for determining when a rate at which said incrementing signals are received falls below a selected minimum value; and second comparator means responsive to the timing means for providing an indication when the counting means holds a number differing from the random number by less than a predetermined amount when the rate at which the poker machines are played is below said minimum value.

2. An apparatus according to claim 1, wherein the random number is indicative of an amount of money which is paid to a player operating the poker machine which produced said last incrementing signal.

3. An apparatus according to claim 1 or claim 2, wherein the means to generate and store a random number is a counter responsive to a free-running clock, and wherein said counter is started by a reset of the apparatus and stopped by a first incrementing signal from one of the poker machines.

4. An apparatus according to any one of the preceding claims, wherein the indication provided by the second comparator means is an audio and visual indication of encouragement to players of the poker machines.

5. An apparatus according to any one of the preceding claims, wherein optocouplers provide electrical isolation between said poker machines and said apparatus.

6. An apparatus according to any one of the preceding claims, wherein said display means cease to display a prize award indication in the event of a malfunction of the apparatus.

7. An apparatus substantially as herein described with reference to the accompanying drawings.

DATED this 19 th Day of March, 1992

BORIS FRANKOVIC

Attorney: LEON K. ALLEN

Fellow Institute of Patent Attorneys of Australia

of SHELSTON WATERS

ABSTRACT

A random payment awarding apparatus for connection to a plurality of poker machines determines a hidden random prize value and then increments a displayed monetary value by weighted amounts at each operation of the connected poker machines. The apparatus pays out when the incrementing monetary value equals the random prize value. The apparatus provides audiovisual encouragement to players of the poker machines when the incrementing monetary value is within a predetermined amount of the random prize value and the rate at which the poker machines are played falls below a selected minimum value.

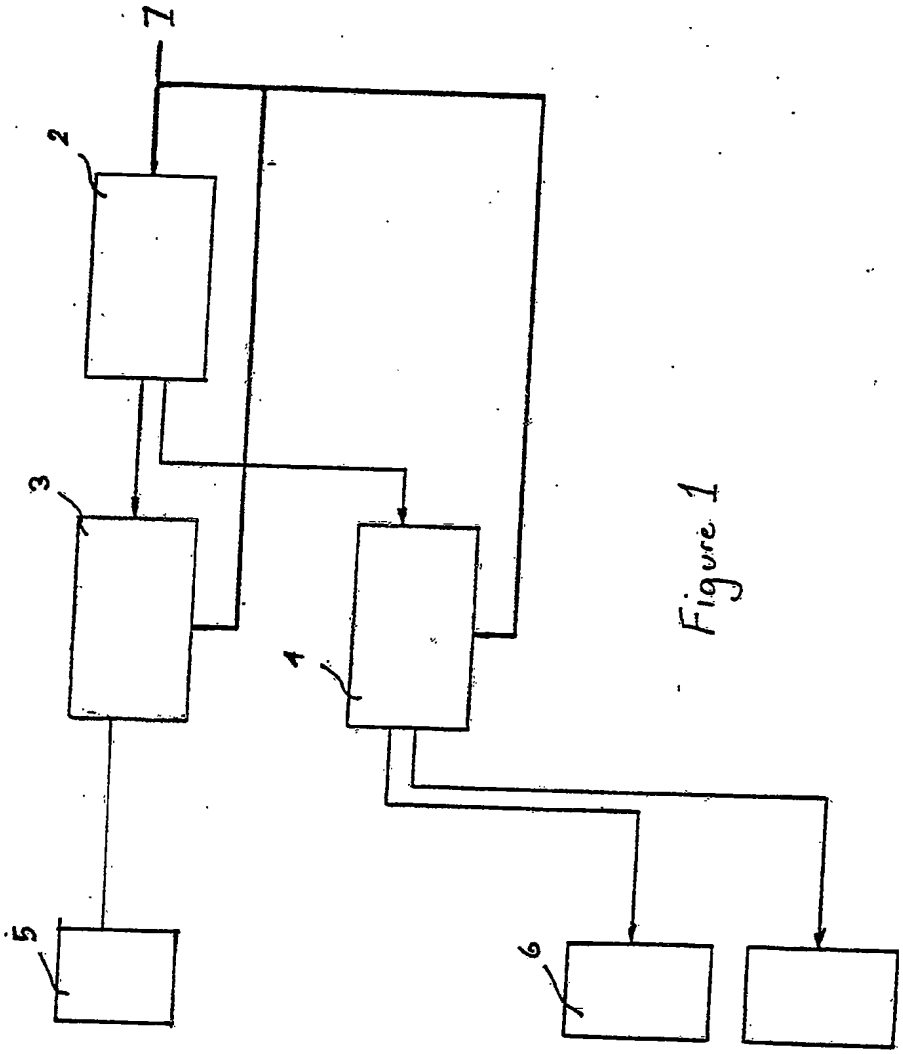
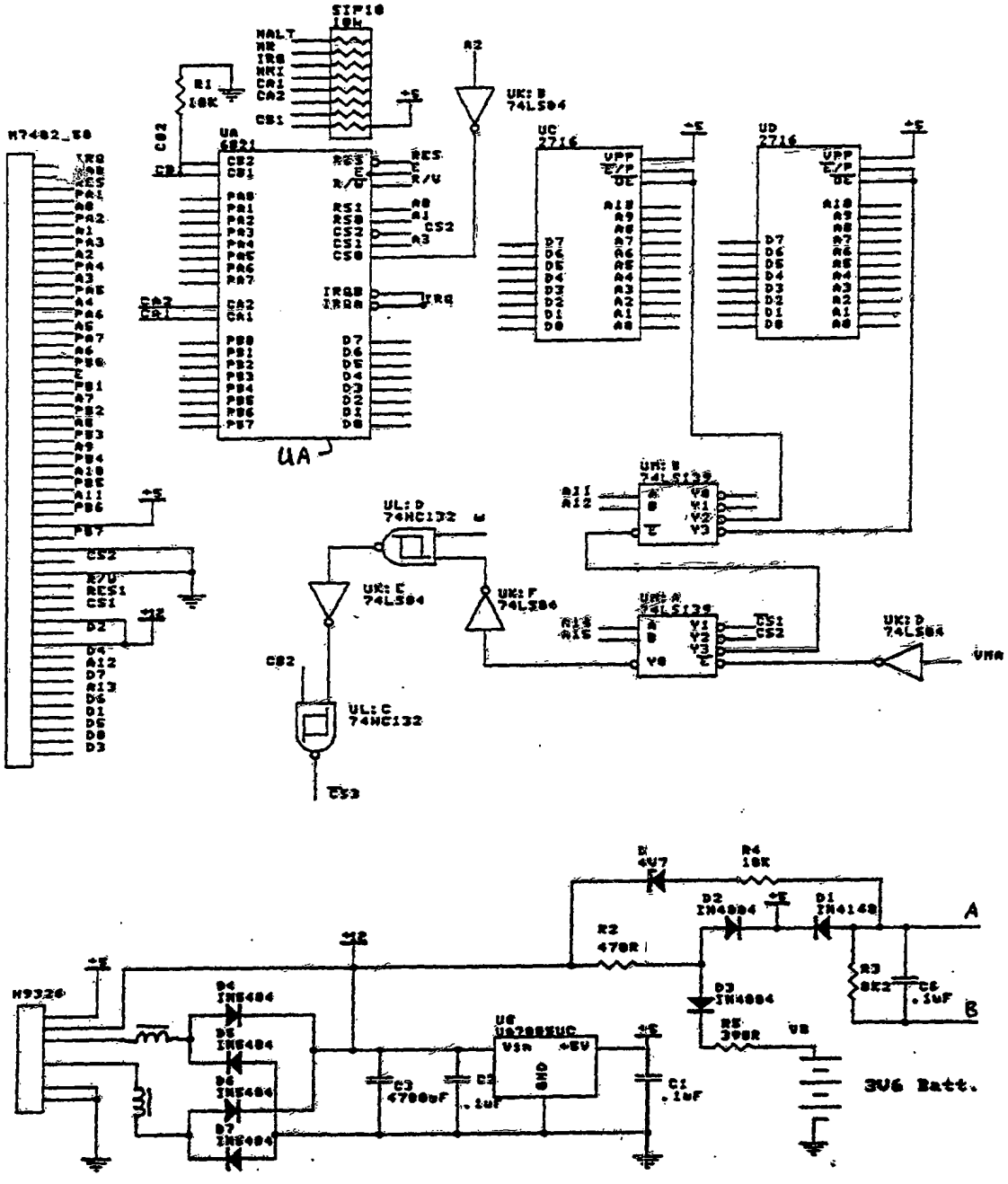


Figure 1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R1
10K
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74LS04
UA
6821
UC
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UD
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74LS139
UL:D
74HC132
UK:E
74LS04
UK:F
74LS04
UL:C
74HC132
UK:D
74LS04
VMA
CS2
CS3
A2
A3
IRQ
+5
+12
H9320
D4
IN5404
D5
IN5404
D6
IN5404
D7
IN5404
C3
4700uF
C2
.1uF
U6
UA7805UC
C1
.1uF
D
4V7
R4
10K
D2
IN4004
D1
IN4148
A
R2
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R3
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C6
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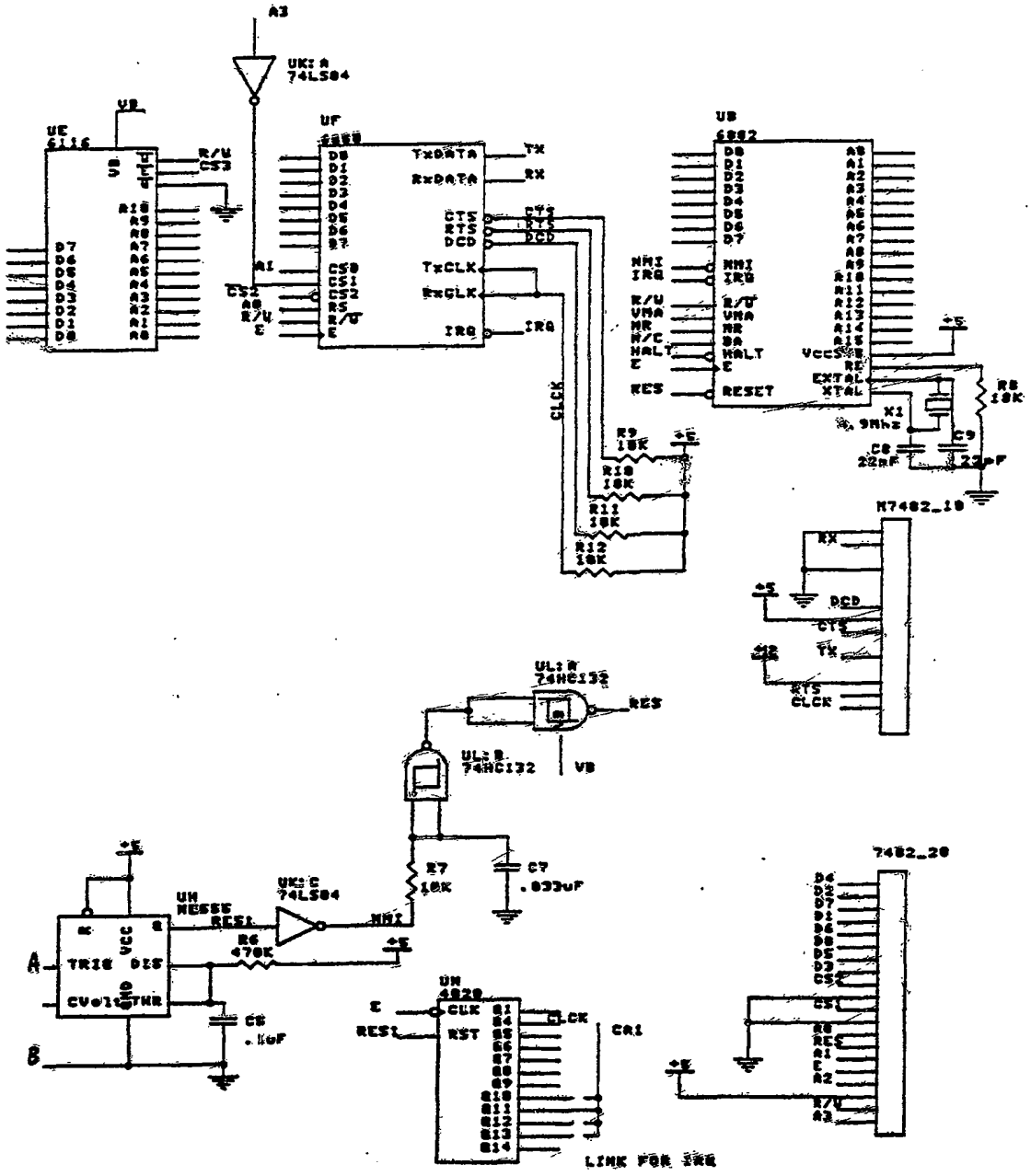
D3
IN4004
R5
300R
VB
3V6 Batt.

FIGURE 2

FIGURE 3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6116
R/W
CS3
A1
CS2
A0
R/W
E
UF
6850
D0
D1
D2
D3
D4
D5
D6
D7
TxDATA
RxDATA
CTS
RTS
DCD
TxCLK
RxCLK
IRQ
TX
RX
CTS
RTS
DCD
IRQ
CLCK
UB
6802
NMI
IRQ
R/W
VMA
NR
H/C
HALT
E
RES
RESET
Vcc
EXTAL
XTAL
X1
9Mhz
C9
C8
22pF
R8
10K
R9
10K
R10
10K
R11
10K
R12
10K
M7402_10
RX
DCD
CTS
TX
RTS
CLCK
U1:B
74HC132
RES
VB
U1:A
74HC132
R7
10K
C7
.033uF
U4:C
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R6
470K
C6
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U3
4020
CLK
RST
CA1
LINK FOR IRQ
7402_20

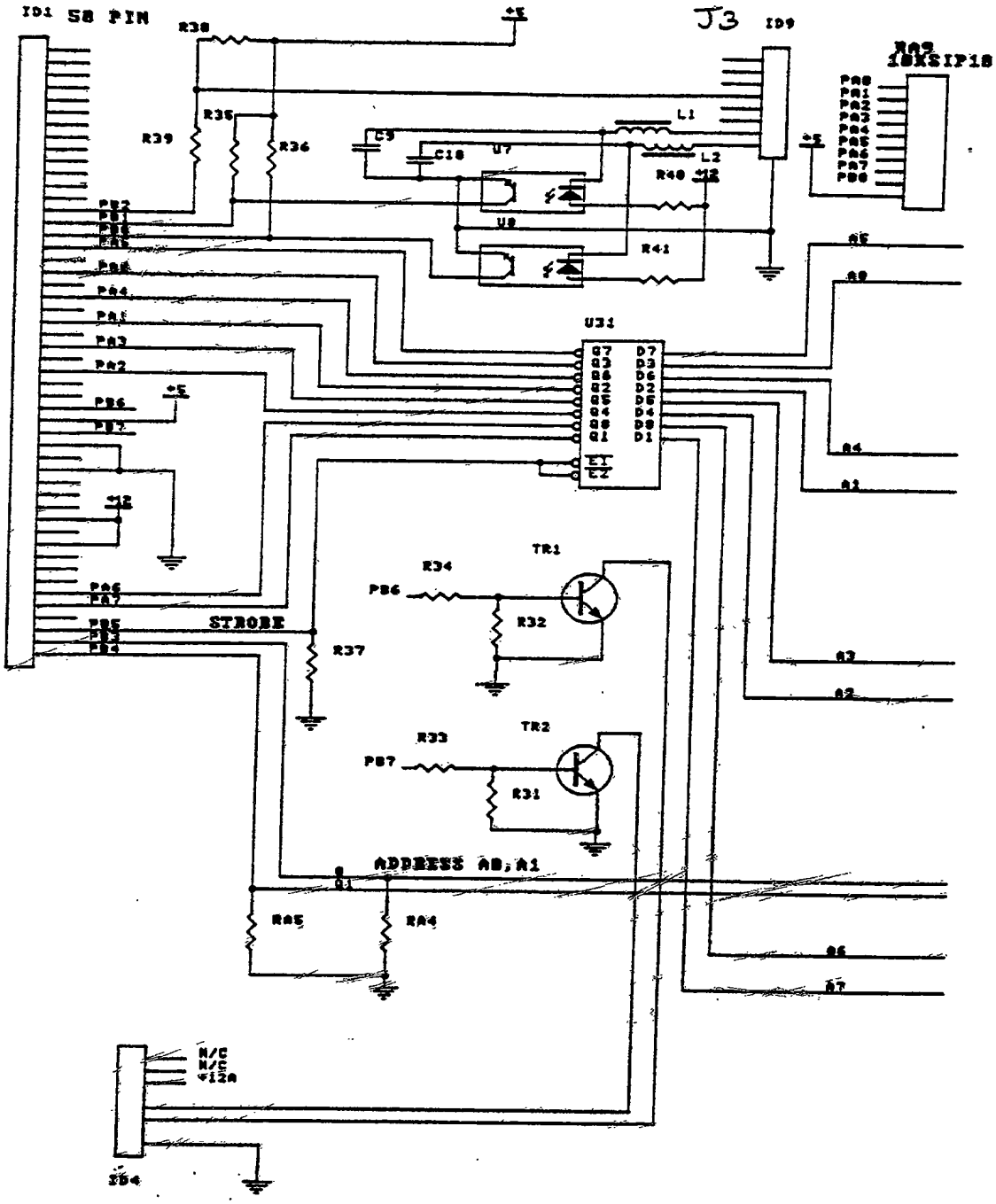
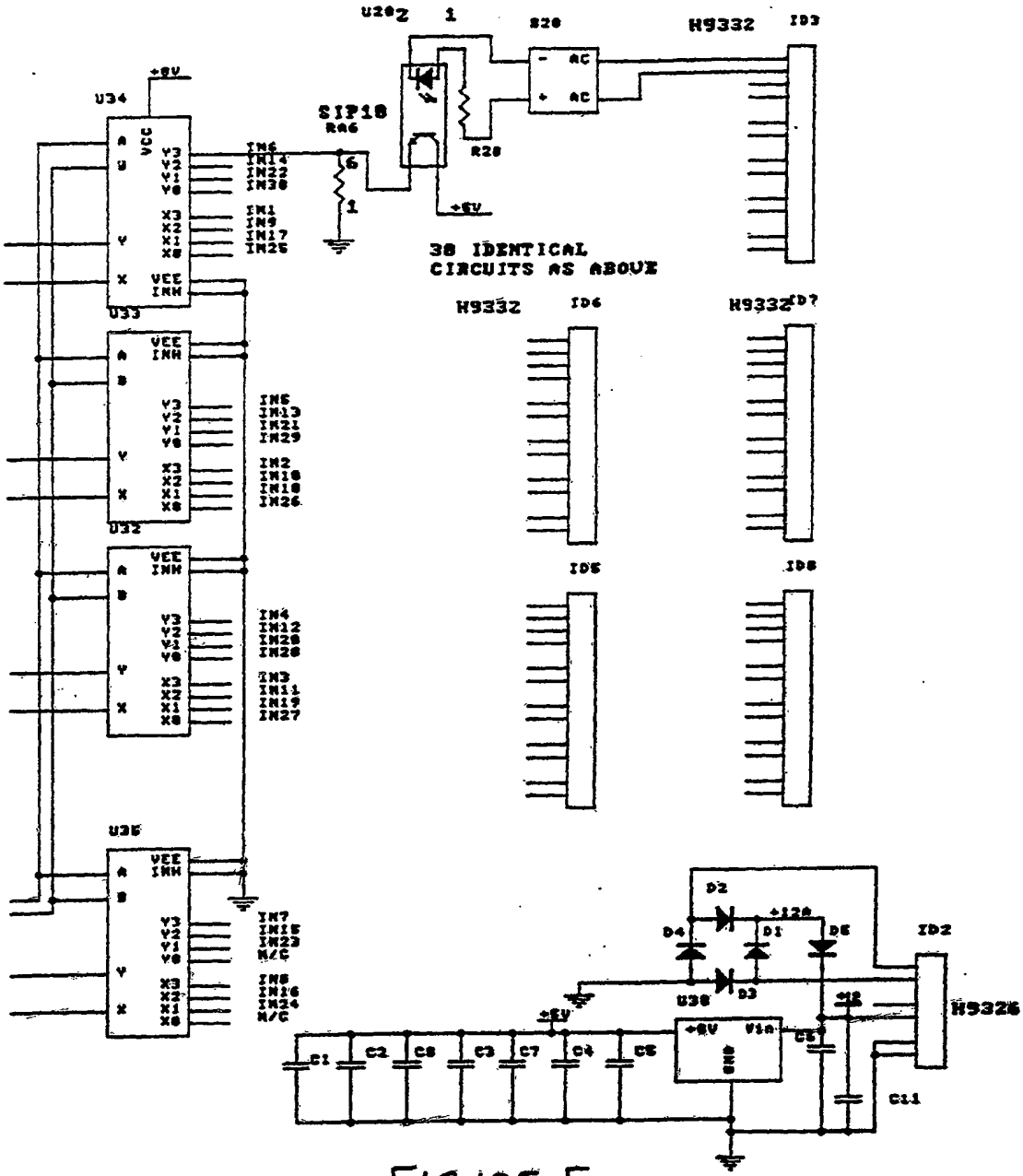

ID1 58 PIN
R38
+5
J3
ID9
RA3
10KSIP10
R35
R39
R36
C9
C10
U7
L1
L2
R40
+12
U8
R41
U31
Q7 D7
Q3 D3
Q6 D6
Q2 D2
Q5 D5
Q4 D4
Q8 D8
Q1 D1
E1
E2
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
A5
A0
A4
A1
A3
A2
A6
A7
TR1
R34
R32
TR2
R33
R31
STROBE
R37
ADDRESS A0,A1
A1
A0
RA5
RA4
N/C
N/C
+12A
ID4

FIGURE 4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U33
U32
U35
SIP10
RA6
R28
U28
S28
H9332
ID3
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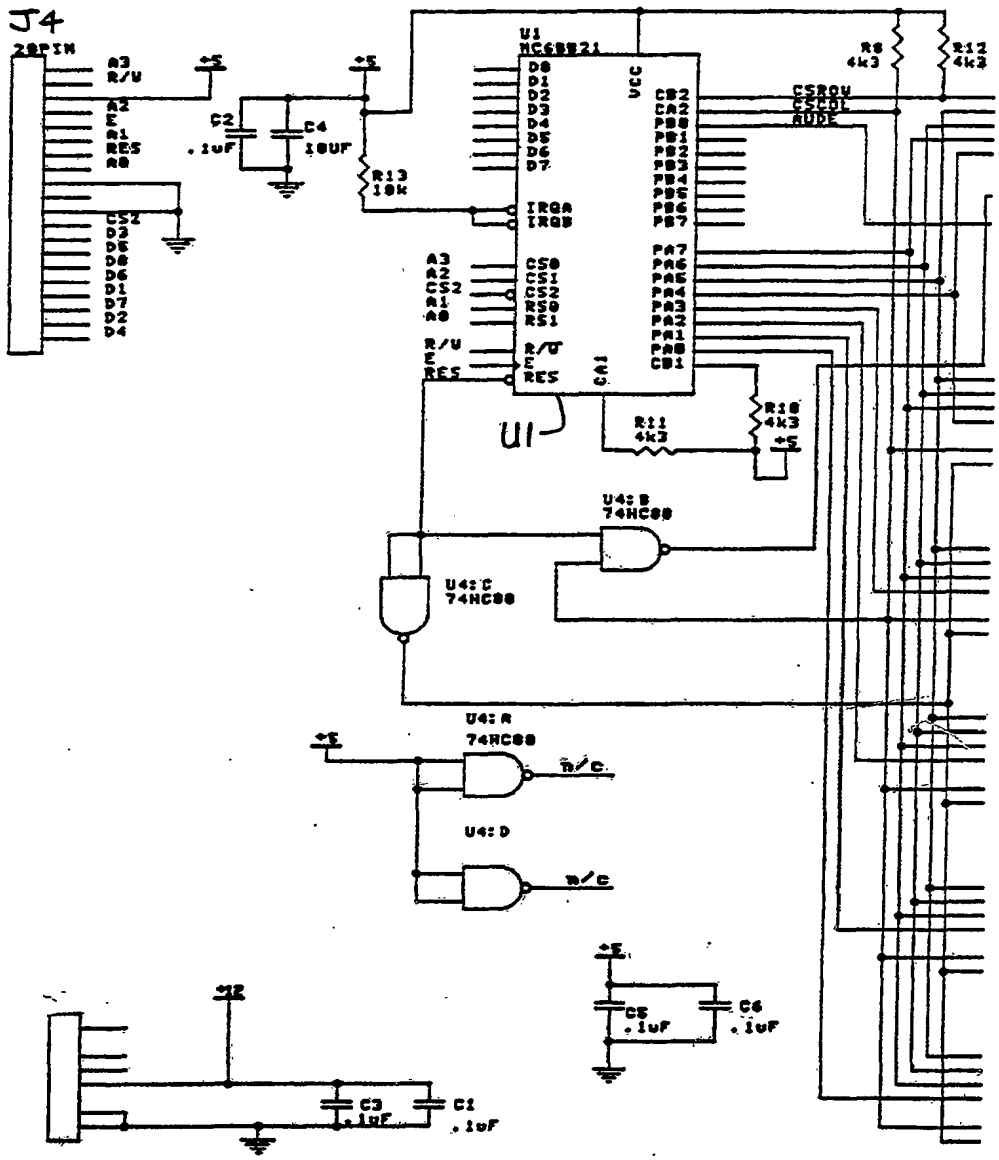
CIRCUITS AS ABOVE
ID6
ID7
ID5
ID8
D2
D4
D1
D5
D3
U38
ID2
H9326
C1
C2
C8
C3
C7
C4
C6
C5
C11

FIGURE 5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28PIN
U1
MC68B21
U1
R13
10k
C2
.1uF
C4
10UF
R8
4k3
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R11
4k3
R10
4k3
U4:B
74HC08
U4:C
74HC08
U4:A
74HC08
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C5
.1uF
C6
.1uF

FIGURE 6

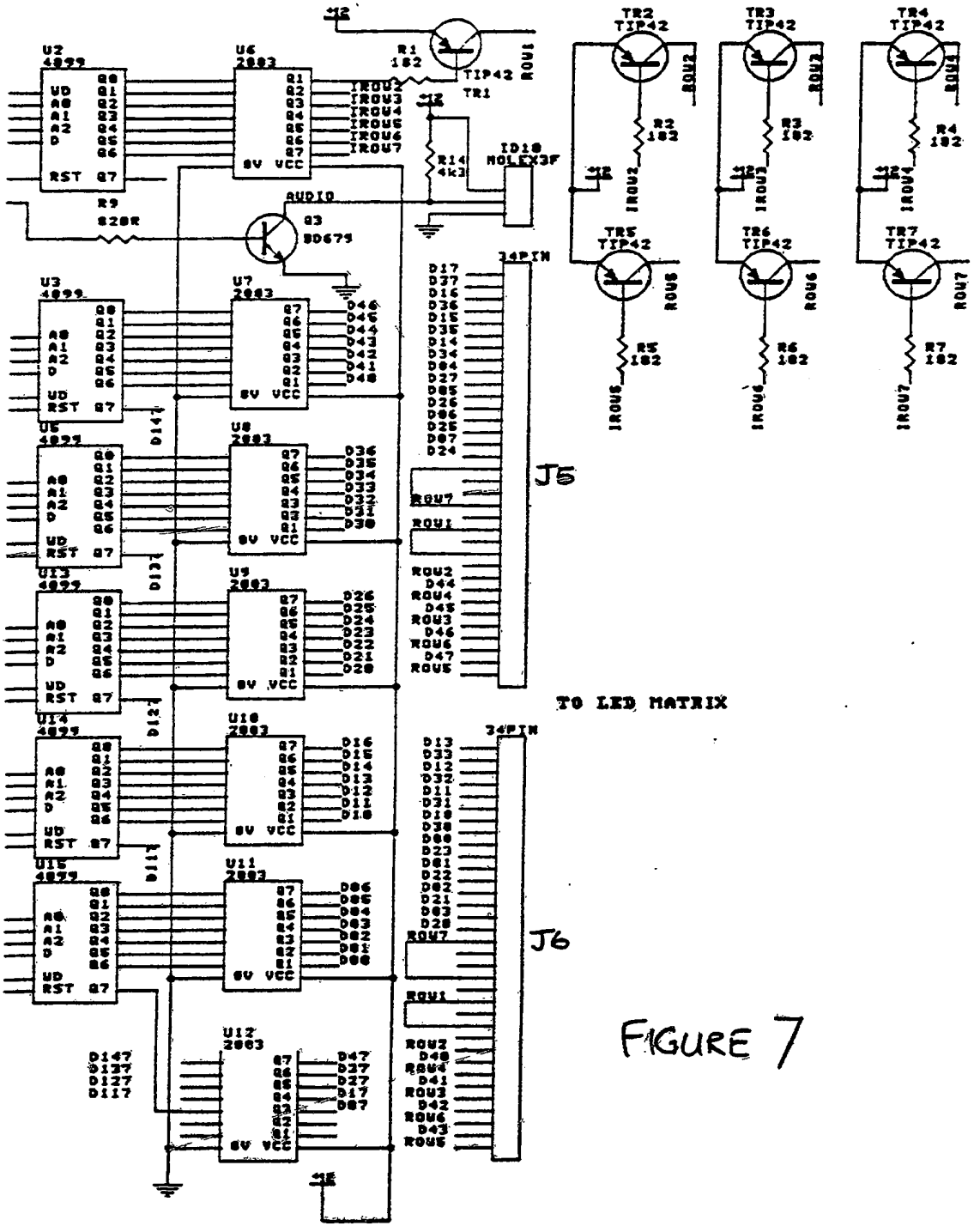
TO LED MATRIX
J5
J6
34PIN
TIP42
AUDIO
BD679
R1 182
R2 182
R3 182
R4 182
R5 182
R6 182
R7 182
R9 820R
R14 4k3
ID18 MOLEX3F
TR1
TR2
TR3
TR4
TR5
TR6
TR7
U2 4099
U3 4099
U5 4099
U13 4099
U14 4099
U15 4099
U6 2003
U7 2003
U8 2003
U9 2003
U10 2003
U11 2003
U12 2003

FIGURE 7